



## Product Type: ASC/3 Controller

### Logic Processor – Yellow + Red Before Green

Reference: AN2075

Date: July 13, 2007

The Peoples Republic of China and other countries around the world sometimes utilize a Yellow and Red signal as an indication that the signal on an approach is about to change to Green. This function can be implemented in an ASC/3 Controller by utilizing the Logic Processor.

The Yellow + Red function is timed and controlled by the **terminating** phase Red Clearance time setting. This yields a signal indication sequence of Red - Red & Yellow – Green –Yellow – Red for the selected phase(s). This approach does require knowledge of the intersections phasing (Ring Structure) and desired Yellow plus Red timing values before programming the Logic Processor and controller.

For this example we will assume a typical 8-phase intersection in a Dual-Quad configuration with the Yellow plus Red indication on the Main Street phases, 2 and 6. The desired operation is to have 2-seconds of Yellow and Red before the phase 2 and 6 signals change to Green. The Logic Processor programming is as follows:

#### Step 1:

```
IF Phase Next 2 is ON  
AND Ring 1 Red Timer (is) > 0  
THEN Set Yellow Phase 2 ON
```

#### Step 2:

```
IF Phase Next 6 is ON  
AND Ring 2 Red Timer (is) > 0  
THEN Set Phase Yellow 6 ON
```

Lastly, program the Red Clearance time for phases 1, 3, 4, 5, 7 and 8 in MM-2-1 to 2-seconds.

In the above example, the first step (#1) checks if the desired phase (2) is going to Time Next, AND checks if Red Clearance is currently timing (Ring 1 Red Timer > 0). It then turns the phase 2 Yellow Phase output ON while the Ring 1 Red Timer is greater than 0-seconds. The second step repeats the process for phase 6 on Ring 2.

It should be noted that the MMU in the cabinet **must** have its option switches for Field Checking and Dual Indication set to OFF for phases 2 and 6 to prevent the MMU from sensing a Dual Indication Fault when the Red and Yellow come on together. Since Field Checking will be disabled on the MMU for these phases it is strongly recommended that Color Checking on the ASC/3 be enabled at least for phases 2 and 6 in this example.

If the Yellow plus Red function is to be implemented on a Time-of-Day basis it may be accomplished simply by enabling or disabling the appropriate Logic Processor Steps. When the Logic Processor steps are disabled the ASC/3 will continue to time the longer Red Clearance times programmed in MM-2-1. If the longer times are not desirable then two Timing Plans must also be implemented to adjust the Red Clearance times as needed.



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Due to the potential variability of Red Clearance Timing at an intersection this Logic Processor sequence may not be suitable for use in the “hidden area” (above step 100) with an EXT file since both the Logic Processor programming and the Red Clearance timing may need to be changed to correctly implement any desired reduction or increase of the Red Clearance time and Yellow plus Red time. However, placing the programming in the upper numbered steps can obscure the programming from a casual observer while still allowing modification from the controller keyboard. When placing the programming in the upper steps be aware of the processing sequence restrictions for the Logic Processor. Refer to the base ASC/3 Logic Processor Programming Application Note for further details.